Application Note **MSAN-148**

An Introduction to MVIP™ and Details on Implementation using the MT90810

CONTENTS

ISSUE 1 September 1994

1.0 MVIP

1.1 An Overview

MVIP (Multi-Vendor Integration Protocol) provides a coherent approach to building solutions for worldwide markets by merging computing and communications technologies under one open architecture. MVIP ensures interoperability among telephone-based resources (such as, trunk interfaces, voice, video, fax, text-to-speech, speech recognition) for use within a computer chassis in an individual or networked configuration. The architecture is both supported and driven by an industry-wide group of over 200 companies worldwide who are licensees of the MVIP technology.

1.2 The History

Mitel Semiconductor initially defined ST-BUS (Serial Telecom Bus) to provide an effective means of communication and information transfer between functional modules. The required interface to this bus was designed into new ST-BUS compatible components such as the digital switches and the phone chips. As telecommunications and computer technologies merged, it was not long before applications for the devices grew to include the personal computer (PC). Now, there was a requirement to provide a means of communication between physical cards within a PC chassis. Based on the ST-BUS interface and the associated clocks and signalling, the MVIP bus was developed.

MVIP is a vendor-independent standard; thus the name “multi-vendor”. The MVIP standard was cooperatively developed by a group of companies, including Mitel, to address the problem of interoperability in today’s call processing environment. Today, MVIP is a widely deployed industry standard that ensures interoperability and simple integration of multiple technologies from different vendors.

1.3 The Purpose

MVIP provides a framework within which manufacturers of computers and communications systems can plan hardware and software products, complete systems and customer solutions to meet current market demand and future market directions. Its broad-based, worldwide adoption by

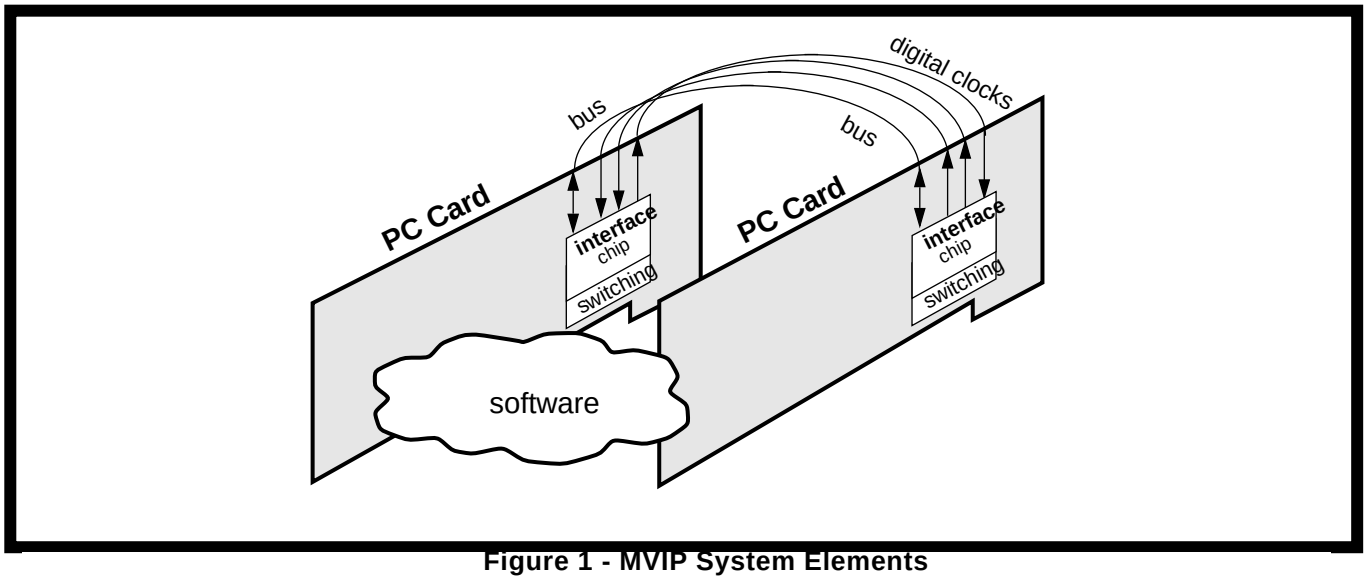

Figure 1 - MVIP System Elements

manufacturers and systems developers provides a proven, extensible platform upon which end-users can plan implementation of their near-term and long-term telephony-enhanced solutions.

1.4 The Architecture

The MVIP architecture specifies the following five integral elements: a bus, switching, digital clocks, software and an interface chip.

- **MVIP Bus**

  The MVIP Bus is a standard digital telephony bus that permits connections of different technologies within a PC chassis.

  The MVIP Bus consists of 16 2.048 Mb/s serial streams - eight DSi streams and eight DSo streams and associated clock signals. 32 channels, of 64 kb/s each, are time division multiplexed onto one DSi/DSo stream. The direction of a DSi/DSo[1] channel-pair is uniquely determined. Therefore, any combination of input and output channels may be multiplexed onto a single DSi/DSo stream. The complete MVIP bus, however, will always carry a total of 256 input channels and 256 output channels or 256 full-duplex channels (refer to Figure 2 - “The MVIP serial streams”).

  The serial streams may be referred to as MVIP streams or ST-BUS streams as they are electrically compatible with Mitel’s ST-BUS specification for inter-chip communications. Application Note MSAN 126, the ST-BUS Generic Device Specification (Rev.B), provides a detail explanation of the ST-BUS.

  The MVIP Bus carries serial streams between PC boards via a 40 pin ribbon cable allowing PC cards to exchange information directly. The bus therefore opens the PC architecture to voice, video, and data applications that would otherwise over burden the PC processor with data transfers. The MVIP bus is equivalent to an extra backplane that is capable of routing circuit switched data.

- **MVIP Digital Switching**

  The MVIP architecture supports advanced distributed digital circuit-switching within the PC under software control. Switching capacity is distributed amongst MVIP-compatible boards. MVIP defines three levels of switching. In order of increasing capabilities, they are:

  MVIP Switching Compatible

  A device or board that is MVIP Switching Compatible is capable of making full-duplex connections. It may provide interface to only a subset of the complete MVIP Bus. The switch may be blocking but is capable of connecting any channel to an MVIP channel and driving a local channel from an MVIP channel.

  MVIP Standard Switching Compliant

  A device or board that is MVIP Standard Switching Compliant is capable of making full-duplex connections. It must provide interface to the complete MVIP Bus. The switch may be blocking but is capable of connecting any channel to an MVIP channel and driving a local channel from an MVIP channel.

1. A DSi/DSo channel pair refers to a channel x (x = {0,1,2,....31}) on DSi stream n (n={0,1,2,....7}) and its corresponding channel x on DSo stream n.

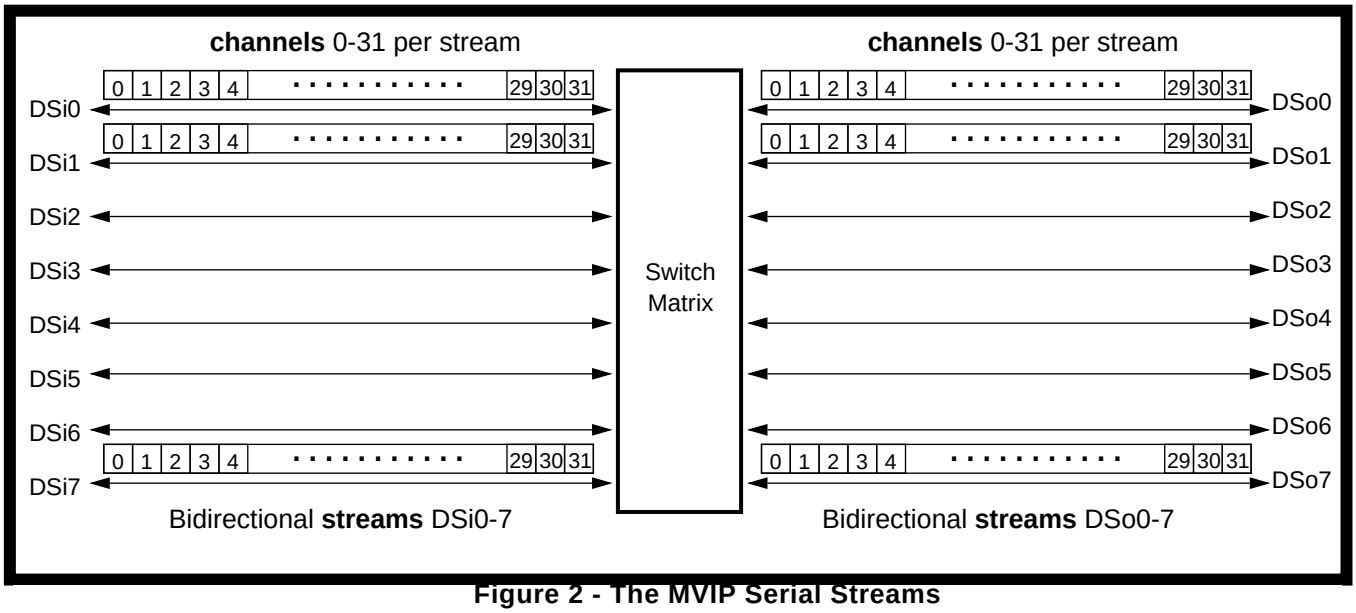

Figure 2 - The MVIP Serial Streams

MVIP Enhanced Switching Compliant

A device or board that is MVIP Enhanced Switching Compliant is capable of making full-duplex connections as well as providing per channel pair direction control for all 256 MVIP channel pairs on the MVIP Bus. It must, therefore, provide interface to the complete MVIP Bus. It is a 256x256 non-blocking switch.

- **MVIP Digital Clocking**

  In an MVIP system, the clock source chosen to drive the MVIP bus and clock signals is called the master clock. The master clock must source the following three clocks: $\overline{C4}$(4 MHz), C2(2 MHz) and $\overline{F0}$(8 kHz framing signal). All the timing signals are passed across the MVIP Bus from the master clock, configured upon power-up, under software control.

  A device or board that provides a network interface function should be capable of driving the MVIP clock lines, that is, become a master clock. The choice to drive or receive MVIP bus clock signal is selectable, either at installation time or under software control.

- **MVIP Software**

  In addition to hardware standards, MVIP defines a software interface standard to access MVIP hardware elements such as switching and MVIP clock timing. The standard specifies functionality independent of programming language.

MVIP software standards include a Connection Control Standard which describes a collection of software entities that cooperate to establish and terminate circuit-switched connections between multiple devices, multiple MVIP cards, and mutiple expansion buses, across one or more computer chassis (refer to Section 1.4.1 Multi-chassis MVIP for details).

The standard specifies the services and objects to be provided by an Application Programming Interface (API) in order to allow connections to be established and terminated in an abstract fashion.

These services include making and breaking connections, configuring a network of MVIP cards, and monitoring and maintaining the status of all connections.

MITEL's Connection Master^{TM} is a software product that implements the Connection Control Standard. Connection Master is a tool for designers of PC systems who use a variety of MVIP cards in their systems. Connection Master interacts with circuit switches on multiple MVIP cards to make connections and resolve switching contention. Connection Master supports multi-chassis MVIP by allowing resources to be distributed throughout a network. Furthermore, it interfaces between applications and makes connections in such a way that simple, one chassis applications become networked applications.

- **MVIP Interface Chip - MT90810**

  Mitel's MT90810, the Flexible MVIP Interface Circuit (FMIC), provides a cost-effective solution to a complete MVIP compliant interface between the MVIP bus and a wide variety of processors, telephony interfaces and other circuits. The MT90810 is specifically designed to meet the switching requirements of the MVIP Bus. Device details may be found in the MT90810 datasheet.

1.4.1 Multi-chassis MVIP

MVIP is an architecture for scalable interconnection and switching of telephony traffic between computer nodes. Multi-chassis MVIP supports interconnection of MVIP chassis and facilitates interoperation with and between other buses. The multi-chassis architecture includes a standard Connection Control API. It provides for common software control of alternative physical media (see Table 1). It supports bus, ring and star interconnection topologies.

As an example, Figure 3 shows an implementation of multi-chassis MVIP using Mitel's FIM.

1.5 Potential for Growth

MVIP provides the potential and opportunity for powerful growth. MVIP specifies a multi-chassis architecture for scalable interconnection and switching of telephony traffic between computer nodes. It defines a comprehensive switching fabric that can be reconfigured as systems grow from board to multi-board as well as chassis to multi-chassis. Multi-Chassis MVIP supports the interconnection of MVIP-based computer chassis, as well as MVIP chassis with other chassis supporting any variation of n x 64 kb/s traffic.

Furthermore, MVIP focuses on easy inter-operation with existing equipment and therefore provides an interface implementation to assist interconnection to proprietary equipment.

1.6 Products in the Market

MVIP allows developers and end users to provide a broad range of MVIP compatible board-level products, end-user products, systems and integrated solutions. Driven by market demand, the MVIP community has been creating new products thus continuously expanding the existing base of products. To date, thousands of MVIP compatible products have been shipped by MVIP licensed companies.

2.0 MT90810 (FMIC)

2.1 An Overview

The MT90810, otherwise known as the Flexible MVIP Interface Circuit (FMIC), is a MVIP (Multi-Vendor Integration Protocol™) compliant device. It provides a complete, MVIP interface between the MVIP Bus and a wide variety of processors, telephony interfaces and other circuits.

The MT90810's built-in digital time-slot switch provides MVIP Enhanced Switching between the full MVIP Bus and any combination of up to 128 full duplex local channels of 64 kb/s each. An 8 bit microprocessor port allows real-time control of switching and programming of device configuration. The device, with its enhanced switching capability, is well suited for use in distributed systems whereby all resources may have switching capability and do not have to rely on a central switching resource.

The MT90810's internal clock circuitry, including both analog and digital phase-locked loops, supports all MVIP clock modes. The device is therefore able to provide glitch-free clock reconfiguration in the event of a network failure by synchronizing to an alternate network reference source.

The MT90810's local serial interface supports PCM rates of 2.048, 4.096 and 8.192 Mb/s, per channel message mode, an additional control stream, as well as parallel DMA through the microprocessor port.

Link name	Link type	Number of 64 kb/s timeslots	Maximum number of chassis supported	Maximum distance
A mesh of T1 or E1 or other point-to-point links				
MC1	Twisted-pair copper	1408	20	15 metres
MC2	FDDI-II fiber or copper	1536	hundreds	many kilometres
MC3	SDH/SONET fiber	2400/4800	hundreds	many kilometres
Mitel FIM	TDM over fiber	256	limited	2 kilometres

Table 1 - Physical Implementations of Multi-Chassis MVIP (MC-MVIP)

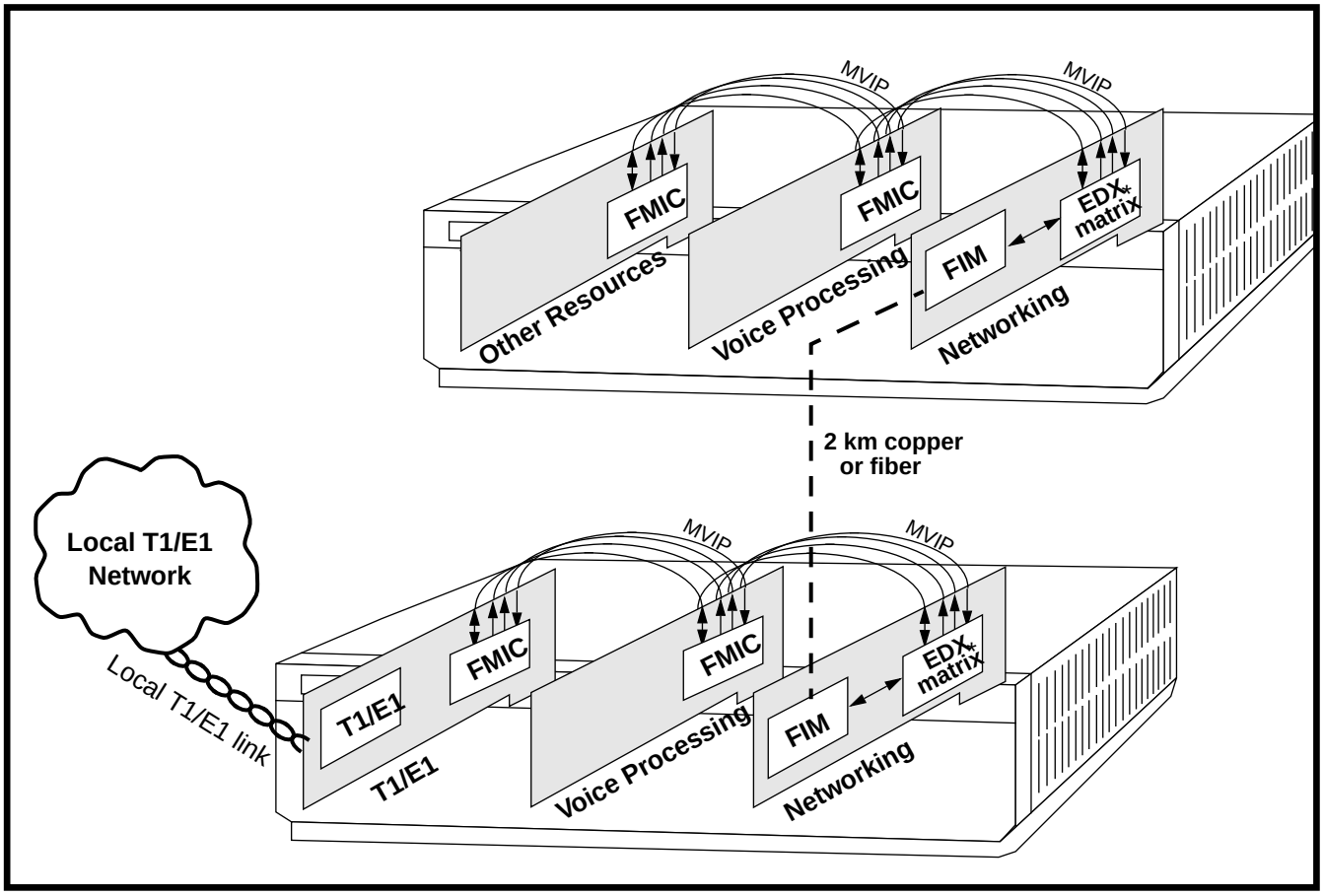

Figure 3 - A Typical Implementation of Multi-Chassis MVIP

* Note: A detailed illustration of the EDX Matrix can be found in the MT8985 datasheet.

Furthermore, the device's programmable group of output framing signals and local output clocks may be used to provide the appropriate frame and clock pulses to drive other local serial buses such as GCI.

The MT90810 is designed for applications where voice and data samples are encoded into individual 64 kb/s timeslots. For such applications, the MT90810 allows cost effective implementation of a non-blocking 384 channel switch. The MT90810 facilitates the implementation of a complete MVIP interface.

2.2 MT90810 Support circuitry

Figure 4 - "MT90810 Support circuitry" shows the MT90810 with suggested support circuitry:

The DSi and DSo I/Os are connected to the MVIP connector through series 47ohm resistor networks. The MVIP clock and framing signals connect directly to the device. The R-C terminations for the MVIP clock lines are jumper-selectable, as specified by the MVIP Standard.

The buffered microprocessor bus and interface signals from the PC interface connect directly to the MT90810. In this example, ALE is grounded to put the MT90810's microprocessor interface in INTEL non-multiplexed mode. The ERR pin may be used to generate interrupts to the PC.

The MT90810's DMA interface readily operates with an external DMA Controller to provide DMA transfers for all the local channels. The local interface, local output clocks and programmable framing signals may be used to interface to other devices.

A four pin header provides access to the JTAG pins of the MT90810 for boundary scan board connectivity testing.

Inset A shows a PLL interface circuitry:

A 16.384 MHz crystal is connected across the crystal oscillator pins X1 and X2. This crystal oscillator provides a time base for the MT90810 when it is programmed to become a timing master of the MVIP bus.

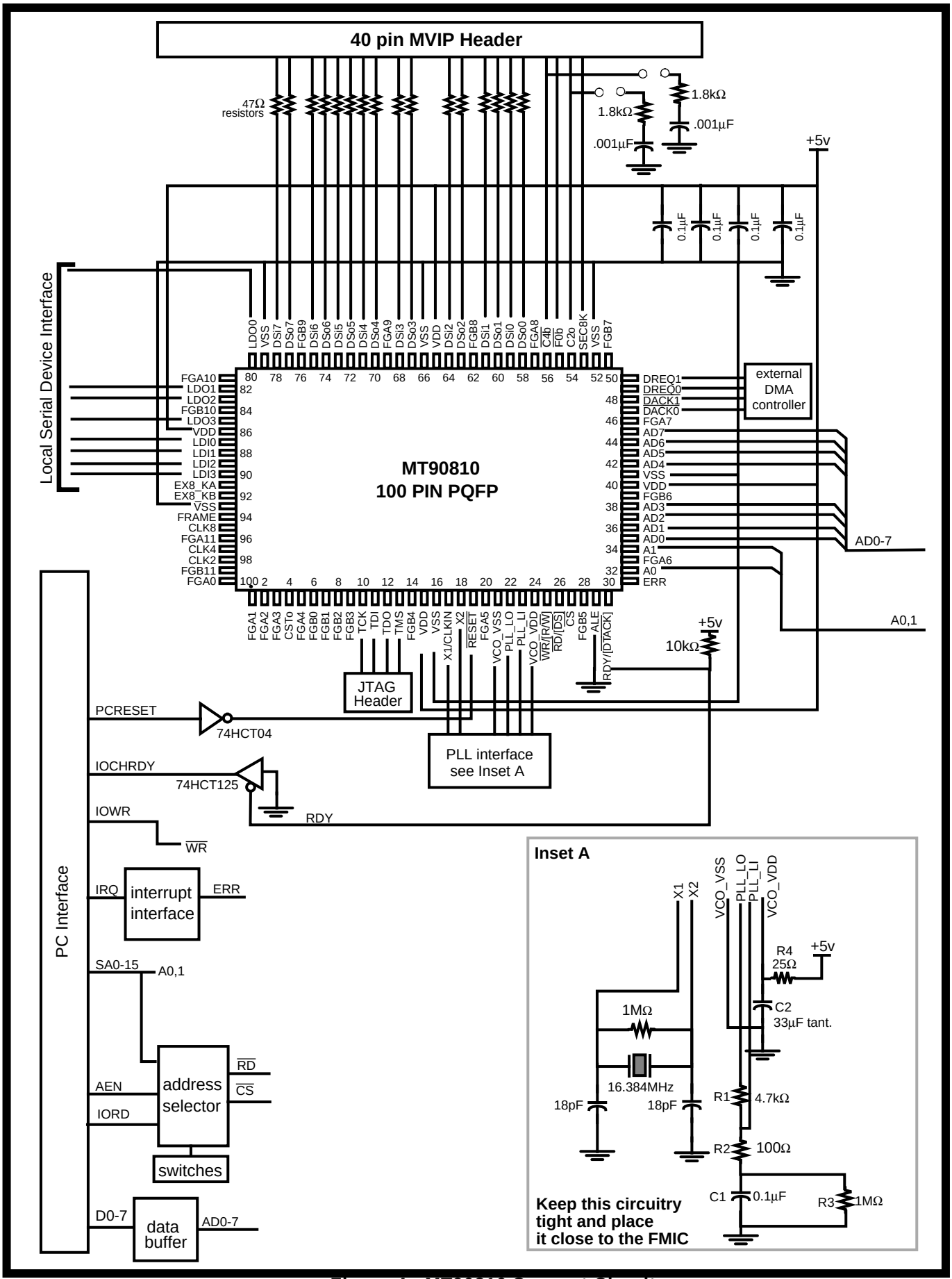

Figure 4 - MT90810 Support Circuitry

R1, R2, R3 and C1 make up a standard lead-lag loop filter for the phase lock loop circuitry of the MT90810. The VCO on the MT90810 has an extremely high gain of about 20 MHz per volt. Consequently, the components making up the loop filter should be placed as close as possible to the MT90810.

The MT90810 internal VCO is modulated by variations in the VCO power supply. Consequently, the VCO power supply is heavily filtered by R4 and C2. This low pass filter eliminates high frequency power supply fluctuations. Low frequency fluctuations can be tracked by the response time of the loop filter.

2.3 Distributed Switching Advantage

The MT90810 enables a system designer to create a distributed switching system easily and cost effectively.

Central Switching

In a central switching system, resources can only transmit to and receive from other resources through the central switching resource. That is, two channels are used to establish a single channel communication link between the resources - one from the resource to the central switch and another from the central switch to the resource. Furthermore, broadcasting data to various resources is inefficient since the application must duplicate the data on a different channel for each resource and bandwidth is costly.

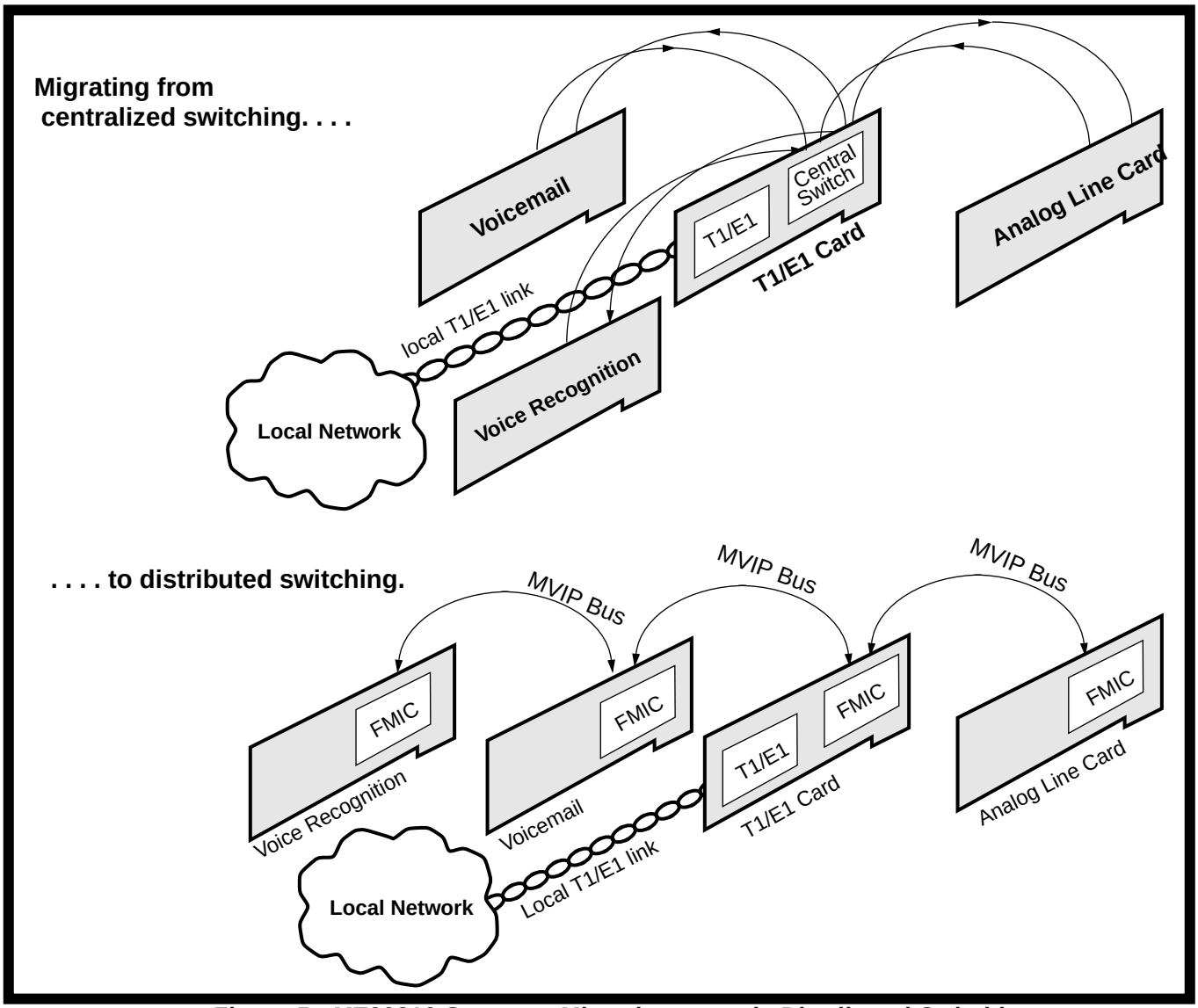

Figure 5 - MT90810 Supports Migration towards Distributed Switching

Distributed Switching

Distributed switching eliminates dedicated switching resources and allows for more flexibility and extensibility in system configuration. In a distributed switching system, resources can transmit to or receive from any other resource without depending on a central switching resource. Switching is reduced to a single stage. Applications can broadcast data efficiently to many resources using a single available channel, thus saving data bandwidth.

2.4 Applications

2.4.1 Glitch-free Clock Reconfiguration

Figure 6 illustrates an application whereby the MT90810 is used to support glitch-free clock reconfiguration in the event of a link failure. As shown, MT90810's MVIP master clock may be programmed to frequency lock to one of three 8kHz timing reference clocks EX8KA, EX8KB or SEC8K. The MVIP master clock is initially frequency locked to the EX8KA, that is the 8kHz extracted from the local T1/E1 link. In the event of a failure on link1, the MT90810 on the Dual T1/E1 Card will remain master of the MVIP bus, but its reference will come from a different source. The MT90810 will frequency lock to EX8KB, the 8 kHz reference derived from the local T1/E1 link2. If then, link2 also fails, the MT90810 on the Dual T1/E1 Card can still remain MVIP master. It can frequency lock to SEC8K, the secondary 8KHz derived from the local T1/E1 link3 passed from the single T1/E1 card over the MVIP bus.

The MT90810 on the Dual T1/E1 card must be set in the PLL modes 1, 2, or 3 (depending on the 8kHz source selected) whereby the PLL is frequency but not phase locked to the external 8kHz. This enables the device to frequency lock to various sources without causing a glitch in its output clocks. The phase difference between the MVIP clocks and the system clocks can be handled by the slip buffer within the MH89760/90B. The MT90810 on the single T1/E1 card must be set to PLL mode 4 so that it can drive the SEC8K clock and be slave to the MVIP bus.

2.4.2 Interactive Voice Response (IVR) System

See Figures 7 and 8.

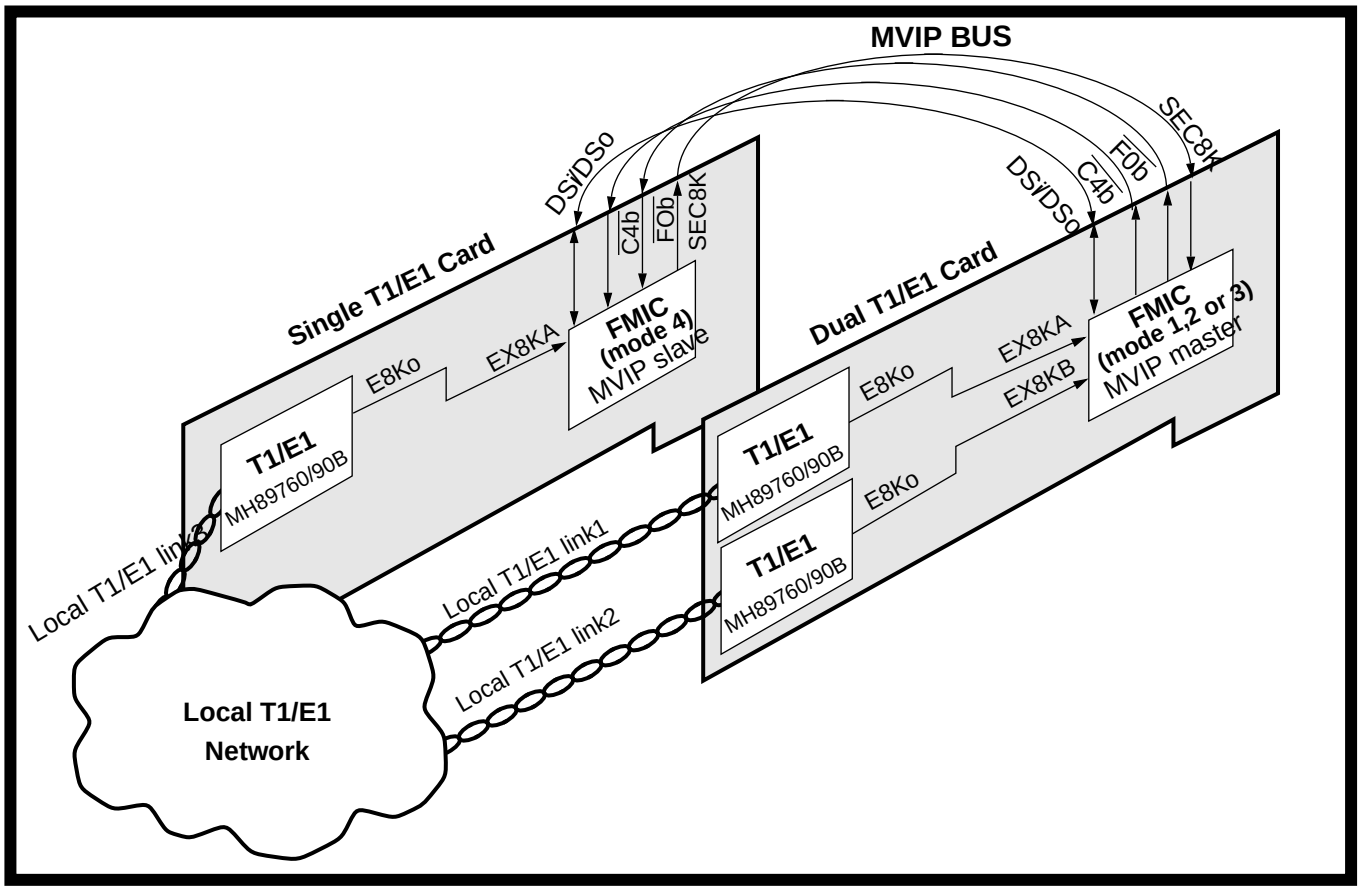

Figure 6 - MT90810 Supports Glitch-free Clock Reconfiguration

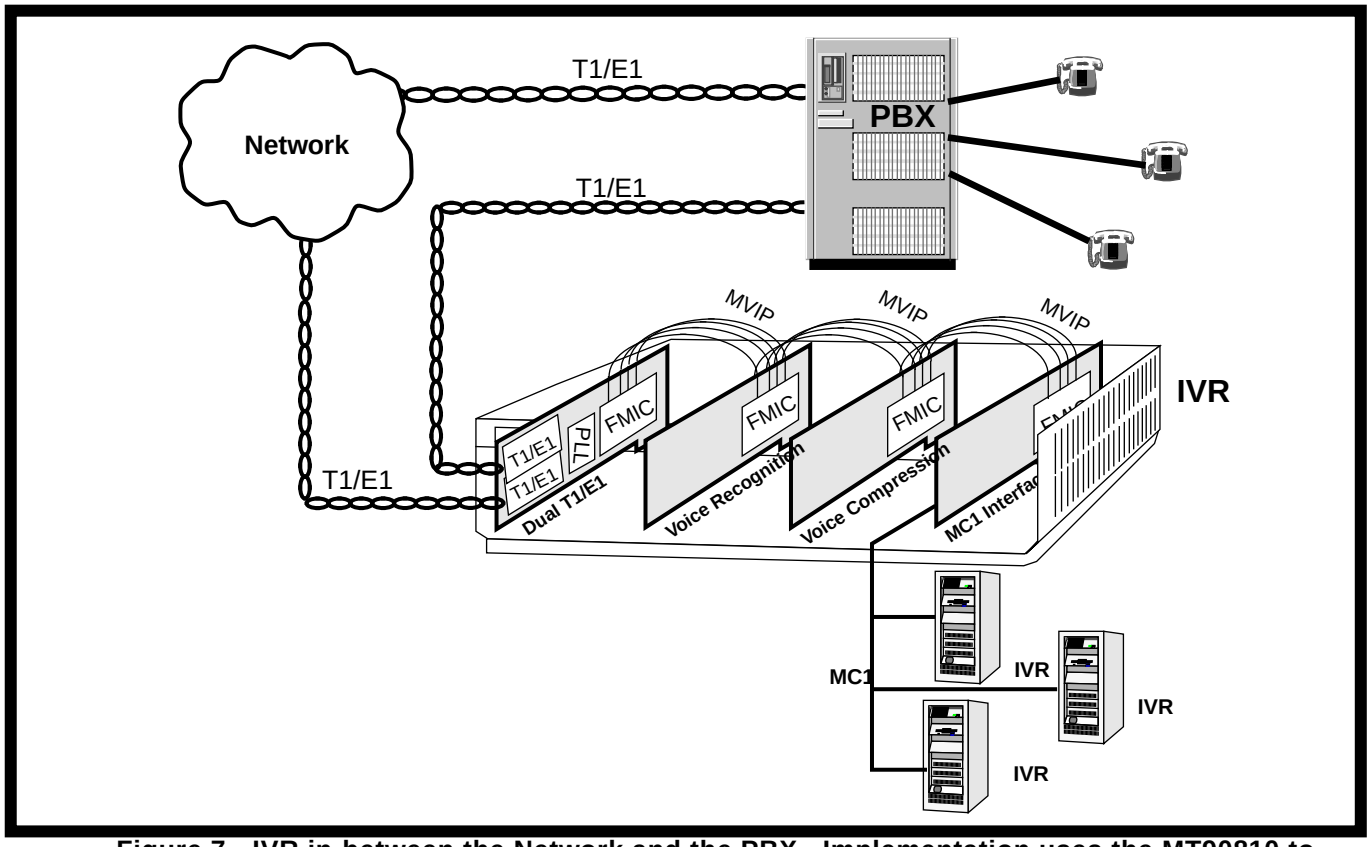

Figure 7 - IVR in-between the Network and the PBX. Implementation uses the MT90810 to provide MVIP interfaces.

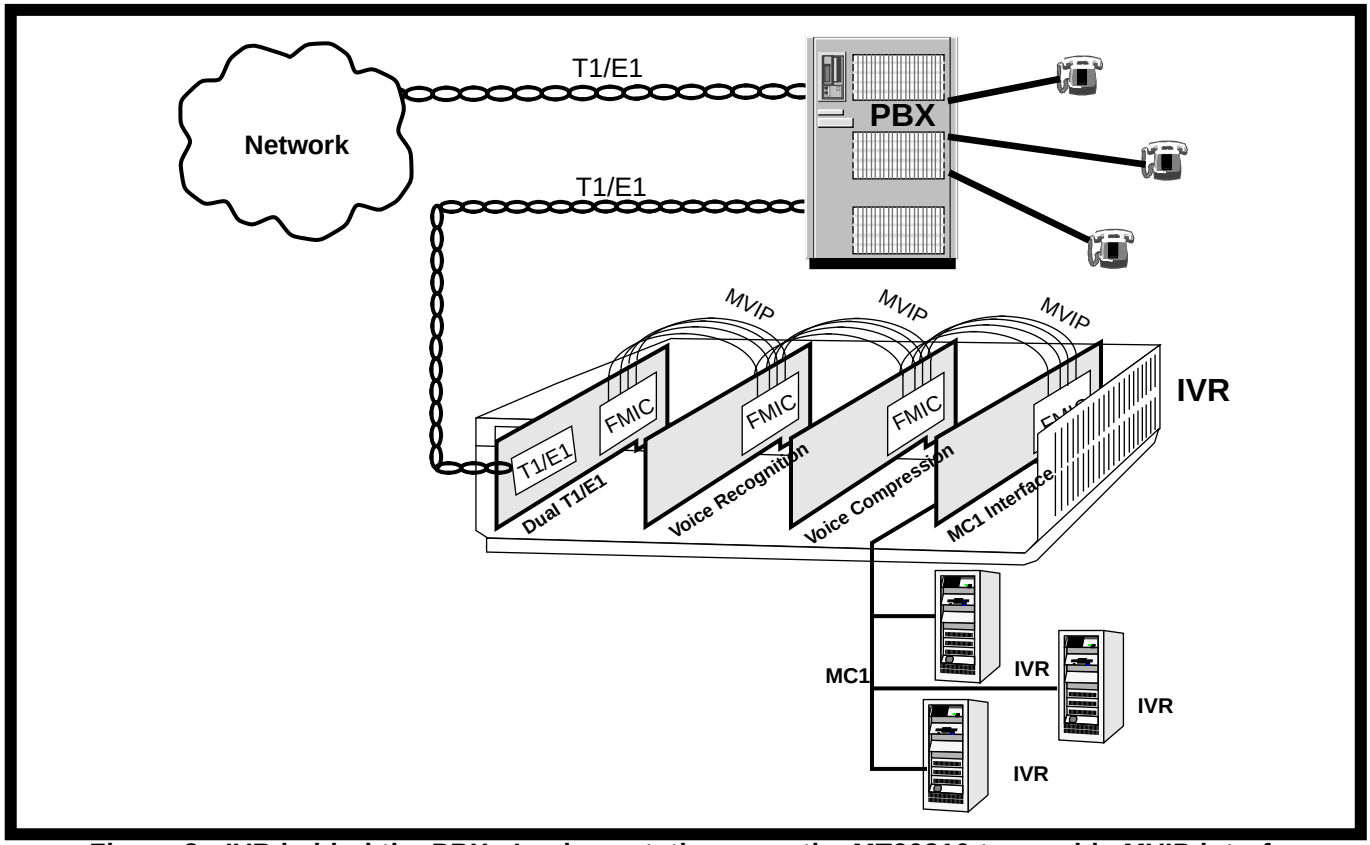

Figure 8 - IVR behind the PBX. Implementation uses the MT90810 to provide MVIP interfaces.

2.4.3 Meeting Network Specifications

The MT90810's digital PLL and analog PLL combination may not meet some international standards for jitter performance. In cases where strict jitter specifications must be met, an external PLL, such as the MT9042 (refer to Figure 9) may be required and the internal analog PLL should be disabled. The MT9042 meets AT&T TR62411 (ACCUNET® T1.5) and ETSI ETS 300 011 specifications for 1.544 MHz (T1) or 2.048 MHz (E1) input reference.

2.4.4 DMA capability

The MT90810's DMA interface readily operates with an external DMA controller to provide DMA for all 128 local channels on it's local serial interface. Figure 10 illustrates an application where the MT90810 is used to send compressed video signals from a video compressor card, via a host bus, out a T1/E1 link. As shown in the illustration, a dual port RAM is required to avoid contention between the DMA controller and the PC host bus.

In this application, the MT90810 is not switching video signals through its switch matrix. Instead, it is performing a fast parallel to serial conversion of compressed video signals for output on the T1/E1 link. Control and signalling can be provided by an HDLC through the MVIP interface. This will require that one MVIP stream be dedicated to perform signalling functions.

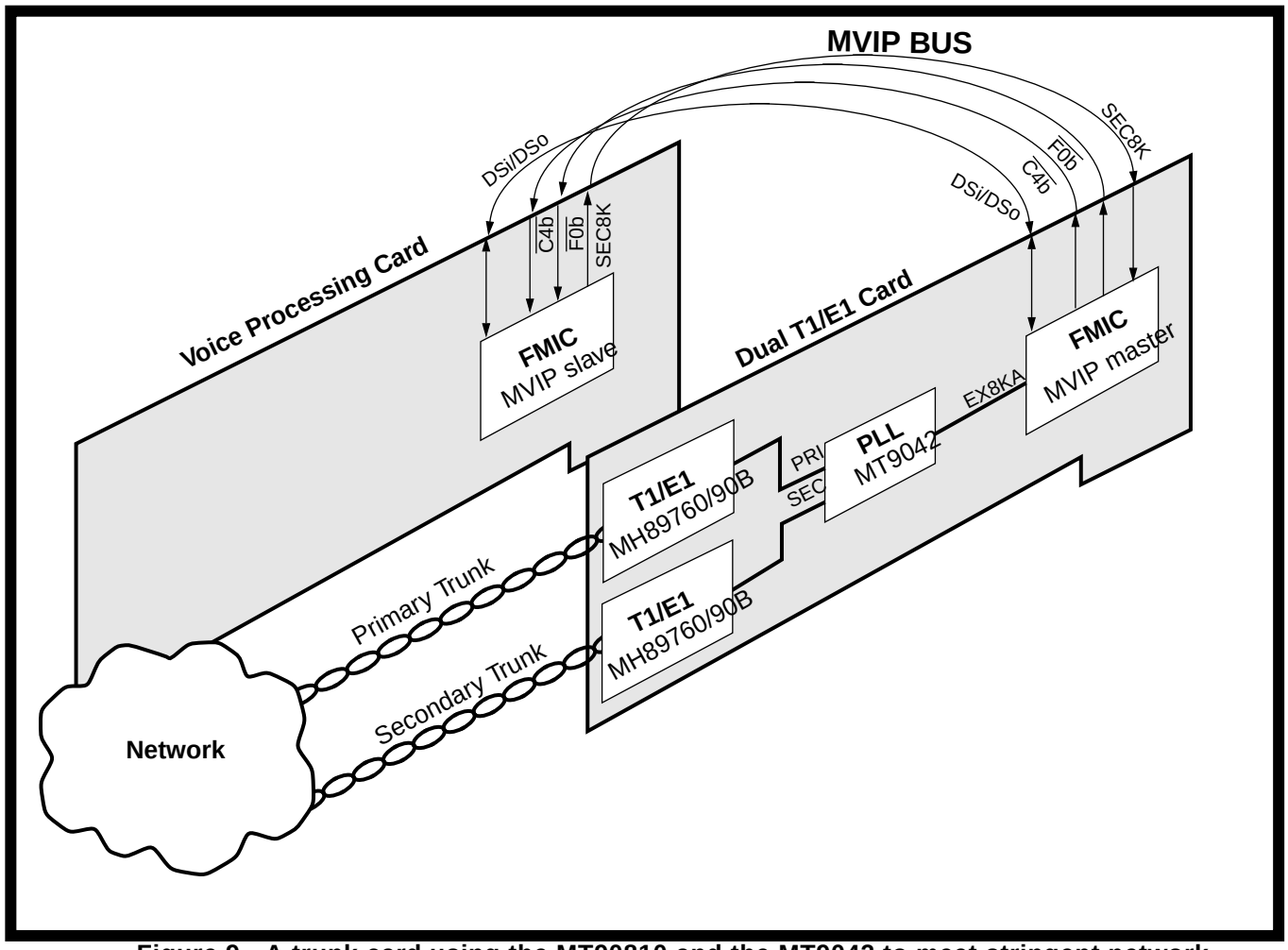

Figure 9 - A trunk card using the MT90810 and the MT9042 to meet stringent network specifications

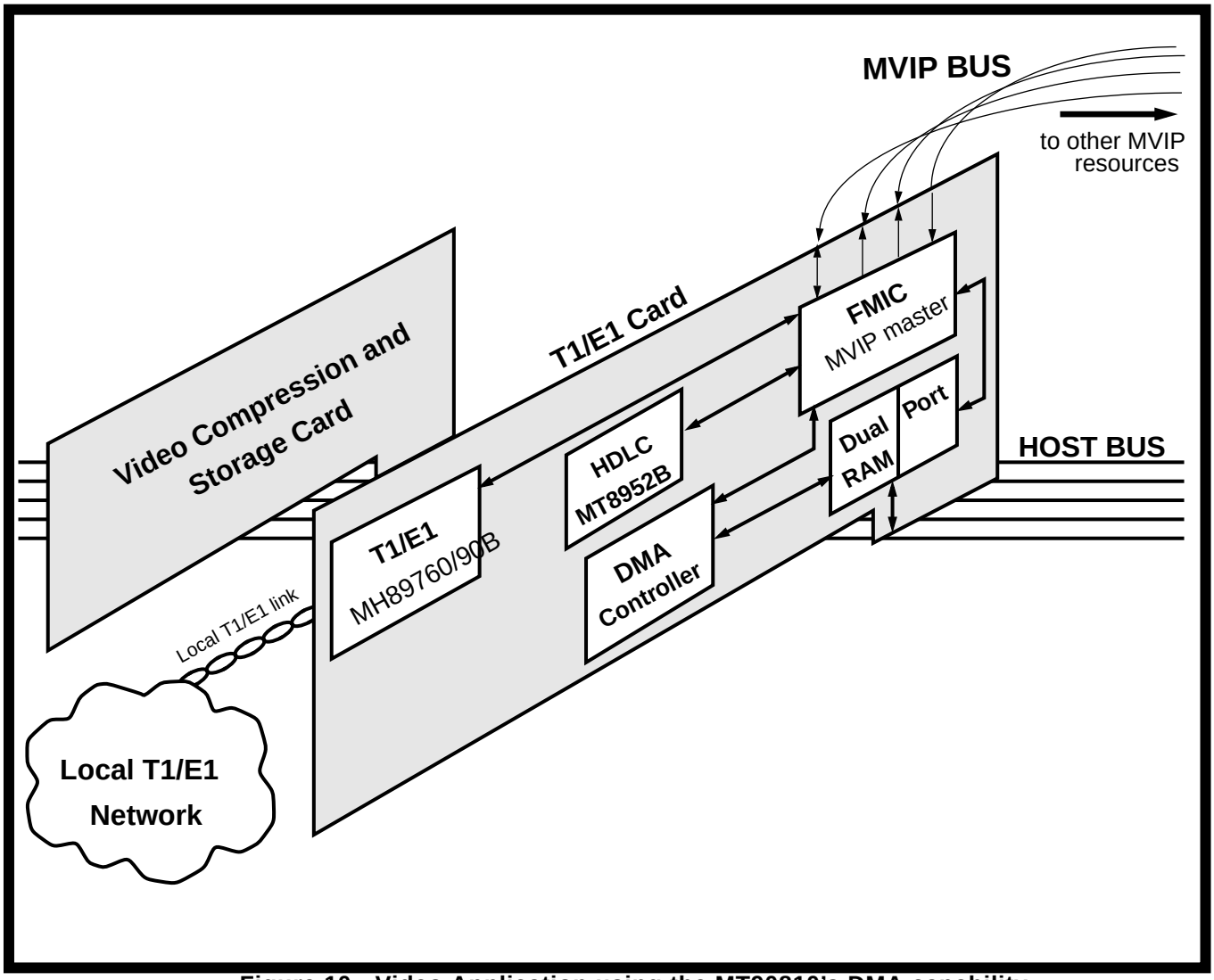

Figure 10 - Video Application using the MT90810's DMA capability

2.5 Device Throughput Delay

A delay through the MT 90810 results when channel information is transferred from one timeslot on an input stream to another timeslot on an output stream. The input information must first be written to data memory, where it awaits the next available timeslot allocated to it for output. The delay is a result of the I/O stages through which data must pass into and out of the device as well as the ordering of memory access cycles.

The MT90810 is a non-blocking switch. This implies that during each timeslot, the device must read and write, to and from, all input and output streams, so that any of its 384 input channels can be switched to any of its 384 output channels. Reading from the input streams involves converting the data from serial to parallel, latching it, then writing into the MT90810s data memory. Writing to the output streams involves reading from the MT90810s data memory, latching it, then converting it from parallel to serial data. The order in which channel information is written into and read from data memory is listed in Table 2, "Memory Access Cycles within a 2 Mb/s timeslot" . As is shown in the table, the device cycles through reads and writes to and from every MVIP and local stream during one 2 Mb/s timeslot. The FMIC state number refers to the number of 16 MHz clock cycles within the 2 Mb/s timeslot. One 2 Mb/s timeslot is 3.9 µs which is equal to 64 16 MHz clock cycles or 64 FMIC states. The connection and data memory runs at half the speed of the FMIC state machine. Memory is therefore accessed every other state.

The I/O stages of the device determine when channel information is written to and read from data memory. Channel information is shifted into the input shift registers during the timeslot allocated to the channel and latched and written to data memory in the timeslot immediately following. Conversely, channel information is always read from data

FMIC State	Memory Access Cycle	FMIC State	Memory Access Cycle
0	MVIP stream 0 write	32	MVIP stream 4 write
2	MVIP stream 0 read	34	MVIP stream 4 read
4	LOCAL stream 0 write	36	LOCAL stream 2 write
6	microprocessor access cycle	38	microprocessor access cycle
8	LOCAL stream 0 read	40	LOCAL stream 2 read
10	MVIP stream 1 write	42	MVIP stream 5 write
12	MVIP stream 1 read	44	MVIP stream 5 read
14	microprocessor access cycle	46	microprocessor access cycle
16	MVIP stream 2 write	48	MVIP stream 6 write
18	MVIP stream 2 read	50	MVIP stream 6 read
20	LOCAL stream 1 write	52	LOCAL stream 3 write
22	microprocessor access cycle	54	microprocessor access cycle
24	LOCAL stream 1 read	56	LOCAL stream 3 read
26	MVIP stream 3 write	58	MVIP stream 7 write
28	MVIP stream 3 read	60	MVIP stream 7 read
30	microprocessor access cycle	62	microprocessor access cycle

Table 2 - Memory Access Cycles within a 2 Mb/s Timeslot

memory and latched for output during the timeslot immediately preceding and shifted out the shift registers in the timeslot allocated.

This ordering of events implies that information entering the MT90810 cannot leave in the same timeslot or in the timeslot immediately following. Information that is to be output in the same timeslot as it is input, relative to frame pulse, will be output in the following frame. Similarly, channel information to be switched to the timeslot immediately following the input timeslot will be output in the timeslot allocated one frame later. Examples of channels being switched to the channels immediately following are: switching from Channel 11 to Channel 12 or Channel 31 to Channel 0 (all independent of stream changes).

The minimum delay that information entering and leaving the MT90810 can experience depends on the data rate selected for the serial streams. For 2 Mb/s data rates, the minimum delay is two 2 Mb/s timeslots. Whether this minimum delay is achievable depends on which streams the channel information enters and leaves on. This is due to the order in which information is read and written into data memory as shown in Table 2. Certain input and output stream combinations will allow channel information to leave two timeslots after the channel information is received (refer to Table 3). Note that the combinations listed all have output stream access occurring after input stream access within a 2 Mb/s timeslot.

Input Stream	Output Stream
MVIP stream 0	MVIP stream 1-7 and LOCAL stream 0-3
MVIP stream 1	MVIP stream 2-7 and LOCAL stream 1-3
MVIP stream 2	MVIP stream 3-7 and LOCAL stream 1-3
MVIP stream 3	MVIP stream 4-7 and LOCAL stream 2,3
MVIP stream 4	MVIP stream 5-7 and LOCAL stream 2,3
MVIP stream 5	MVIP stream 6,7 and LOCAL stream 3
MVIP stream 6	MVIP stream 7 and LOCAL stream 3
LOCAL stream 0	MVIP stream 1-7 and LOCAL stream 1-3
LOCAL stream 1	MVIP stream 3-7 and LOCAL stream 2,3
LOCAL stream 2	MVIP stream 5-7 and LOCAL stream 3
LOCAL stream 3	MVIP stream 7

Table 3 - Input Stream to Output Stream Combinations that can provide the minimum 2 Channel Delay

For 4 Mb/s data rates, the minimum delay is three 4 Mb/s timeslots and for 8 Mb/s data rates the minimum is five 8 Mb/s time slots. Tables 4 and 5 summarize the throughput delay values for output stream access occurring before and after input stream access for various I/O rates. The shaded areas of the tables highlight the minimum delay

Input/Output Rate	m<n	m=n, n+1	m=n+2	m=n+3, n+4	m>n+4
2.048 Mb/s (t.s. = 3.9 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s.	(m-n) t.s.	(m-n) t.s.
4.096 Mb/s (t.s. = 1.95 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s.	(m-n) t.s.
8.192 Mb/s (t.s. = 0.975 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s.

Table 4 - Throughput Delay Values for Output Stream Read occurring after Input Stream Write

Input/Output Rate	m<n	m=n, n+1, n+2	m=n+3, n+4	m=n+5...n+8	m>n+8
2.048 Mb/s (t.s. = 3.9 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s.	(m-n) t.s.	(m-n) t.s.
4.096 Mb/s (t.s. = 1.95 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s.	(m-n) t.s.
8.192 Mb/s (t.s. = 0.975 ms)	1 fr. -(n-m) t.s.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s. + 1 fr.	(m-n) t.s.

Table 5 - Throughput Delay Values for Output Stream Read occurring before Input Stream Write

Notes:
m = output channel; n = input channel
t.s.= timeslot is used synonymously with channel
fr. = 125µs frame

achievable for each I/O rate, under the condition specified.

In summary, delay through the MT90810 is dependent on input and output stream, source and destination channel, as well as, I/O data rate. The device is, therefore, best suited for applications where voice and data samples are encoded into individual 64 kb/s timeslots where maintaining sequence integrity between input and output channels is not required. For applications where concatenated or grouped time slots are used to carry voice, video and/or data, the MT90810 must be programmed correctly, using the tables above, to maintain frame integrity. As an alternative, for applications where the sequence integrity of concatenated N*64 kb/s channels has to be maintained, the MT8985 Enhanced Digital Switch is highly recommended. The device provides per-channel selection between variable or constant throughput delay and is designed specifically for hyperchannel switching.

2.6 Microprocessor Accesses

The MT90810 data sheet specifies a microprocessor fast and slow access time in the table titled “AC Electrical Characteristics - Microprocessor Timing”. The fast t_{ACC} applies to register accesses and the slow t_{ACC} applies to memory accesses. Slow memory accesses occur because the MT90810 only

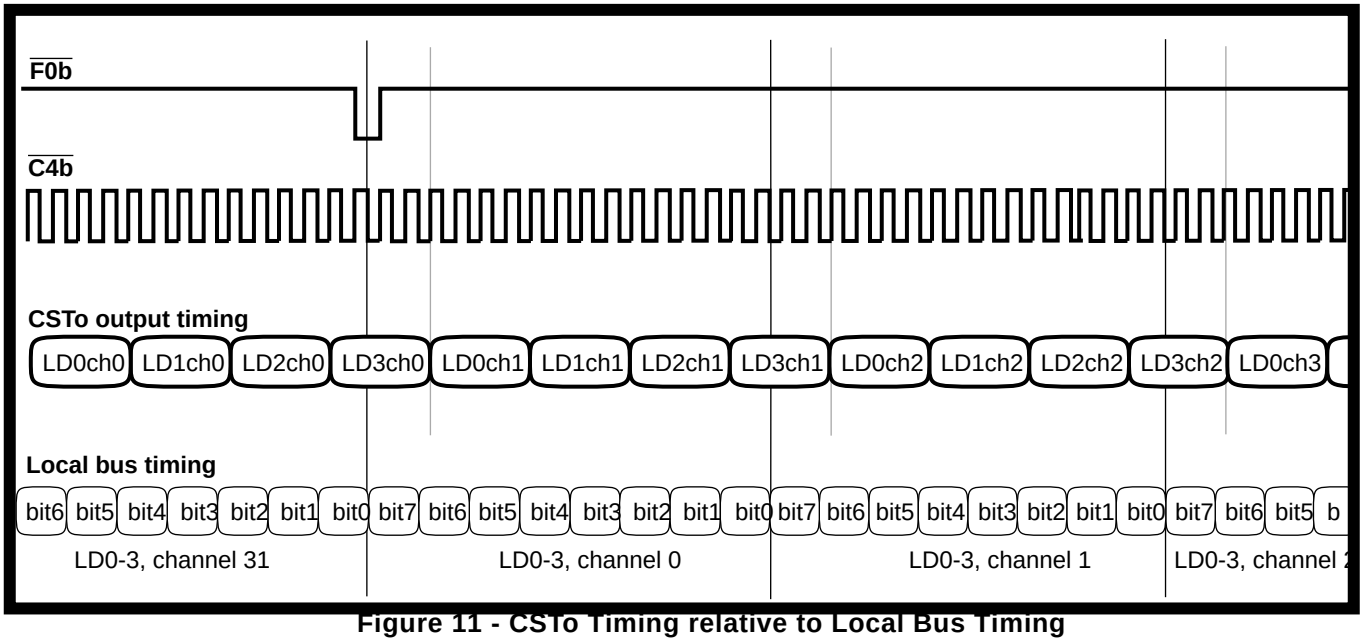

Figure 11 - CSTo Timing relative to Local Bus Timing

allocates discrete access windows for microprocessor memory access. As shown in Table 2, microprocessor access windows occur every four 8 MHz clock cycles (or eight FMIC states). The microprocessor runs asynchronously to the FMIC state machine and must therefore wait until its designated state to access memory.

2.7 External Control Using CSTo

Connection memory high for all 128 local channels includes a CSTo bit. The inverted value of this CSTo bit is output sequentially on the CSTo stream in the order shown in Figure 11 - “CSTo timing relative to local bus timing” . The CSTo stream, like the MVIP streams, is divided into frames that are 256 bits long. Each CSTo bit occupies two bits on the CSTo stream because there are twice as many bits in the stream as there are local channels with associated CSTo bits.

The four CSTo bits that correspond to a channel timeslot are output in the timeslot preceding so that the CSTo bits may perform external control functions, in advance, for the channels they correspond to (see Figure 11). The CSTo bits, for example, may be used to control loop back circuitry. The CSTo stream can enable and disable a driver for a specific channel to be looped back. This function is ideal for performing system level diagnostics and/or delay line applications. The CSTo stream may also be used to sychronize a microprocessor to local stream timing by notifying the microprocessor when a predetermined timeslot in the local stream timing will occur.

3.0 References

Datasheets:

MT9042 Global Digital Trunk Synchronizer

MT8985 Enhanced Digital Switch

MT8980D Digital Switch

MT90810 Flexible MVIP Interface CIrcuit

MT90710 Fiber Interface Mux (FIM1)

MSAN-126 ST-BUS Generic Device Specification (Rev.B).